

TESSENT SUPPORT NOTES

APRIL 2024

Your monthly newsletter with **Tessent** tips and tricks.

Have you ever wondered why the Tessent SSN bus clock and shift clock differ from what you expected?

Tessent SSN automatically determines the maximum clock values according to the ratio of packet size to bus width. See below for a simple example of how Tessent SSN achieves this.



Haitham Nofal
Applications Engineer

✕ [How does Tessent determine SSN bus and shift clock frequencies?](#)

👤 [Tessent on-demand training course](#)

✕ [How to change the TCK frequency?](#)

▶ [Webinar: SSN on-chip compare](#)



Reduce pattern generation time with Tessent LogicBIST - and do more with your day!



Ceci Xie
Applications Engineer

So, you've run Tessent LogicBIST to produce stuck-at patterns—and now want to find LogicBIST transition faults, without regenerating the same patterns? We've got some great articles on fault simulation to help you do this, as well as reduce your overall Tessent LogicBIST pattern generation time.

✕ [How to run fault simulation for LogicBIST transition faults](#)

📄 [White paper: Increase fault coverage & reduce test time with observation scan in your LogicBIST flow](#)



For 1:1 support and suggestions, contact us via the [Support Center](#).

Still have questions? Quiz our experts at our upcoming live webinars.

- 5/14 - Introduction to DFT for tile-based design using SSN - [Register now](#)

Latest release

Download: [Tessent 2024.1](#)



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