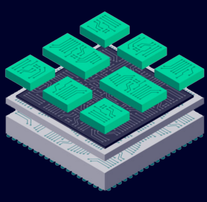
SIEMENS

DIGITAL INDUSTRIES SOFTWARE

The 3D IC multi-physics challenge:

Known good die (KGD) may not behave in 3D IC as stand alone.



What are the 3D IC multi-physic problems?

Passing power generates heat

- Heat propagates slowly through laminate materials
- Need to consider vertical and lateral heat propagation
- Stacking can make access to a heat sink more challenging
  - Heat can also cause changes to EMIR
- Changes in temperature will impact device (transistor) behavior!

3rd dimension and new materials create new stresses

- Impacts of thermal expansion also generate stresses
- Stresses will also impact device (transistor) behavior

Changes in device behavior impact the ability to pass power.

How do you expand from verification to multi-physics analysis?

With electrical reliability analysis from early design to sign-off including:

- Power analysis and EMIR
- Thermal analysis
- Mechanical stress analysis

Power analysis and EMIR

Power integrity analysis for digital, analog, mixed-signal, and 2.5D / 3D IC

What is it?

- Multiple Modes:
  - "-flow analog": GDSII based flow
  - "-flow digital": LEF/DEF based flow
- Electro-Migration and IR-drop analysis for advanced node, 2.5D, and 3D IC analysis

Die Level

- PG Extractor
- Power
- DVD

Package Level

- RLC Extractor
- Die Models Import
- DVD

Thermal analysis

Annotating package-level thermal analysis to the chiplet/IP level

What is it?

- Performs Thermal Analysis
  - Assembly Level
  - Detailed at the Chiplet / IP level
  - Visualization – Color maps, wave forms
  - Back-annotation to spice for later extraction
- Early Design & Sign-off

What are the benefits/value?

- Identify manufacturing issues prior to tape-out
- Optimize designs to enhance yield and manufacturability while reducing cost and scrap

Stress analysis

Annotating package-level stress on chiplets

What is it?

- Mechanical and thermo-mechanical stress analysis
- Analysis levels and results:
  - Assembly level
  - Detailed at chiplet or IP level
  - Visualization - stress and piezoresistive maps
  - Back-annotation to spice for accurate post-assembly electrical simulation
- Early design & sign-off of CPI stress effects

What are the benefits/value?

- Identify manufacturing issues prior to tape-out
- Optimize designs to enhance yield and manufacturability while reducing cost and scrap

Package-scale simulation (FEA)

Output: field of displacement components on the die faces

Die-scale simulation (FEA)

Output: Distribution of the strain components across device layer.

Layout-scale w/ feature-scale resolution (compact model):

Output: Transistor-to-transistor variation in stress components

The keys to addressing 3D IC multi-physics challenge:

- **Single assembly definition across the flow**
  - Planning, design, verification, analysis, post-layout simulation, EMIR
- **Physical and circuit verification**
  - DRC, LVS, PEX … PERC
- **Extended analysis flow**
  - Mpower models feed thermal
  - Mechanical and thermal for stress analysis
  - Stress & thermal results feedback to EMIR
- **Integration commitment to 3rd party integrations**
  - Will integrate to non-Siemens tools as appropriate

What's next?

Discover how Siemens comprehensive chiplet workflows ensure 3D IC packaging success, minimizes disruption, risk, and reduces cost!

Learn more

For more information, visit: siemens.com/3DIC