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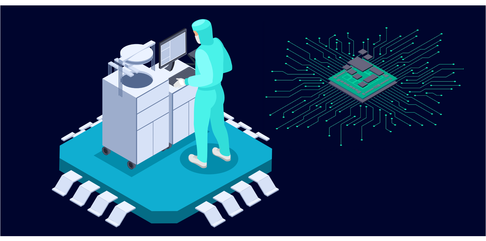
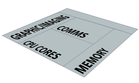
Digital Industries Software

# Why is a comprehensive workflow essential for chiplet design and today's 3D IC architectures?



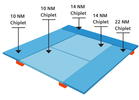
## The Problem: MOORE, is now LESS. Why 3D IC, heterogeneous integration and why the need for homogenous disaggregation?

### Monolithic (SoC)



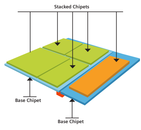

- **Monolithic scaling, as it was traditionally defined, is no longer physically possible.**

### 2.5D Intergration

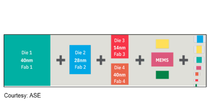



- **We need to meet the silicon demands of advanced applications like AI and high-performance computing**

### 3D Intergration




- **We are trending towards ever-larger chips, as such, we experience increasing yield loss due to their size, and some designs are reaching the reticle size limits.**




Courtesy: ASE


## The Solution: Chiplets

**With today's heterogeneous integration ecosystem, it is now possible to disaggregate large die into multiple chiplets!**

### What's driving chiplets?

**Cost and yield driving alternatives to monolithic solutions**

- SOC disaggregation into hard IP or " chiplet" sub-functions
- Multi-die implementation to avoid reticle limitations (vs. single die)

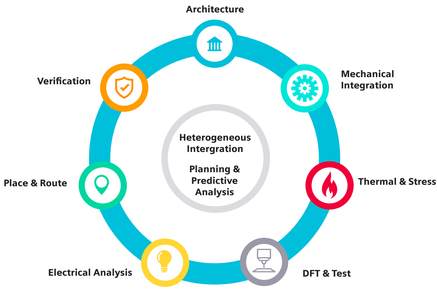
**Data movement - low latency, high-bandwidth**

- Use of High Bandwidth Memory (HBM)
- 3D memory directly stacked on logic
- High-speed, high-bandwidth chip-to-chip interfaces

**Heterogeneous integration provides path forward**

- Supports multiple micro-architecture scenarios
- Leveraging 2.5 and 3D assembly platforms
- Chiplet design-in enablement will drive adoption

## What does the comprehensive chiplet Integration workflow look like?




## Leveraging shift-left technologies is essential to discovering architectural issues in the thermal, mechanical and electrical domains.

**Architecture**
Identify and map chiplets/D2D PHYs to Vendor Libraries
High level power, thermal, throughput analysis
Select appropriate package technology
Capture viable design scenarios
Preliminary floorplan/routing
Assess PPA, cost using co-design/analysis flow

**Verification**
Substrate DRC using PDK
Function verification using LEC
Assembly LVS using ADK

**Place & Route**
3D enabled physical layout of SIP, Chiplet, silicon interposer, and package substrates
Physical IP reuse and concurrent team-based design

**Electrical Analysis**
Parasitic extraction, system level power and timing analysis of die, interposer, and package
Static/dynamic IR drop and electro-migration analysis
Automated interface compliance analysis

**Mechanical Intergration**
Managed co-design of mechanical parts such as stiffeners and heat spreaders with a fully documented ECO flow between ECAD and MCAD. Access to mechanical analysis

**Thermal & Stress**
Thermal analysis from transistorto system-level – chiplet, interposer, package, system. Detailed die-level thermal analysis with accurate package and boundary conditions. Co-simulation and optimization of thermal-mechanical stress effects

**DFT & Test**
Hierarchical DFT, SSN (Streaming Scan Network), enhanced TAPs (test access ports) and IEEE 1687 IJTAG.Scalable, flexibility, and ease-to-use, help designers optimize test technology resources.

## What's next

**Discover how Siemens comprehensive chiplet workflows ensure 3D IC packaging success process that minimizes disruption, risk, and cost!**

**Learn more**

**Key benefits for Siemens 3D IC design flow tools scalable, flexibility, and ease-to-use, help designers optimize test technology resources**

**3D IC digital transformation**
Enable digital transformation for 3D chip design with co-design, co-simulation and automated system analysis and checking. Replace manual interfaces and data exchanges with automated methods and defined workflows.

**3D IC verification and validation**
Comprehensive 3D IC packaging coverage for performance validation and design verification from predictive to final sign off. Automated reviews identify overt issues earlier in the chip design process and eliminate iterations.

**Better 3D IC design resource utilization**
Support team-based design for concurrent development and enable IP reuse and managed blocks. Leverage one chiplet layout tool for organic and silicon substrates for better advanced packaging design.



For more information visit
siemens.com/3DIC